24AA52/24LCS52

2K 2.2V I²C™ Serial EEPROM with Software Write-Protect

Features:

- Single supply with operation down to 1.8V
- Low-power CMOS technology:
  - 1 mA active current, typical
  - 1 µA standby current, typical (I-temp)
- Organized as 1 block of 256 bytes (256 x 8)
- Software write protection for lower 128 bytes
- Hardware write protection for entire array
- 2-wire serial interface bus, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA52) and 400 kHz (24LCS52) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 16 bytes
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP, MSOP and DFN packages
- Pb-free finishes available
- Available for extended temperature ranges:
  - Industrial (I): -40°C to +85°C

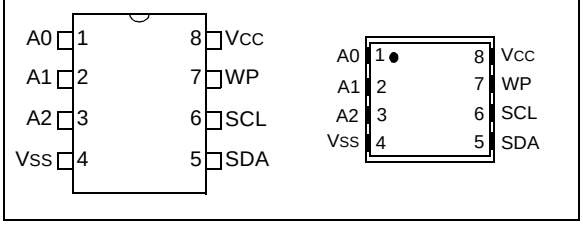
Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA52	1.8-5.5	400 kHz(1)	I
24LCS52	2.2-5.5	400 kHz	I

Note 1: 100 kHz for Vcc <2.2V

Package Types

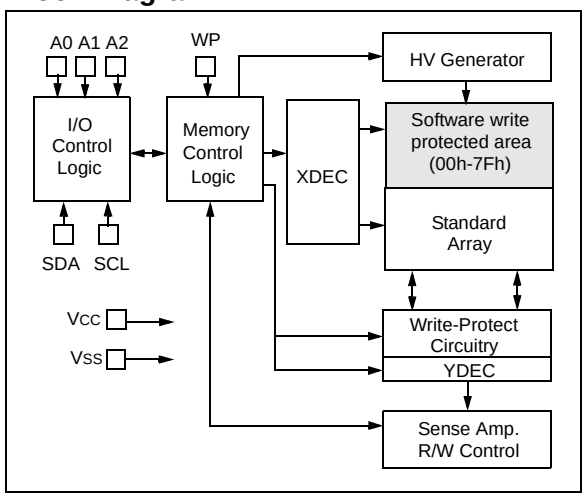
PDIP/SOIC/TSSOP/MSOP/DFN



Description:

The Microchip Technology Inc. 24AA52/24LCS52 (24XXX52*) is a 2 Kbit Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 5.5V). This device has a software write-protect feature for the lower half of the array, as well as an external pin that can be used to write-protect the entire array. The software write-protect feature is enabled by sending the device a special command. Once this feature has been enabled, it cannot be reversed. In addition to the software protect feature, there is a WP pin that can be used to write-protect the entire array, regardless of whether the software write-protect register has been written or not. This allows the system designer to protect none, half, or all of the array, depending on the application. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 µA and 1 mA, respectively. The 24XXX52 also has a page write capability for up to 16 bytes of data. The 24XXX52 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP, MSOP and DFN packages.

Block Diagram



*24XXX52 is used in this document as a generic part number for the 24AA52/24LCS52 devices.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC SPECIFICATIONS

DC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH	A0, A1, A2, SCL, SDA and WP pins	—	—	—	—	—
D2	—	High-level input voltage	0.7 VCC	—	—	V	—
D3	VIL	Low-level input voltage	—	—	0.3 VCC	V	0.2 VCC for VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 VCC	—	—	V	**(Note)**
D5	VOL	Low-level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	ILI	Input leakage current	—	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, FCLK = 1 MHz
D9	ICC write	Operating current	—	1.0	3.0	mA	VCC = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.20	1.0	mA	—
D11	ICCS	Standby current	— —	0.36 —	1.0 —	µA	Industrial SDA = SCL = VCC A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC SPECIFICATIONS

AC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	— —	400 100	kHz	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
2	T_{HIGH}	Clock high time	600 4000	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
3	T_{LOW}	Clock low time	1300 4700	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
4	T_R	SDA and SCL rise time **(Note 1)**	— —	— —	300 1000	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
5	T_F	SDA and SCL fall time	—	— —	300	ns	**(Note 1)**
6	$T_{HD:STA}$	Start condition hold time	600 4000	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
7	$T_{SU:STA}$	Start condition setup time	600 4700	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
8	$T_{HD:DAT}$	Data input hold time	0	— —	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	100 250	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
10	$T_{SU:STO}$	Stop condition setup time	600 4000	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
11	T_{AA}	Output valid from clock **(Note 2)**	— —	— —	900 3500	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
12	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	— —	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
13	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum	20 + 0.1 C_B —	— —	250 250	ns	2.2V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA52)
14	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	**(Note 1 and Note 3)**
15	T_{WC}	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C, V_{CC} = 5.0V, Block mode **(Note 4)**

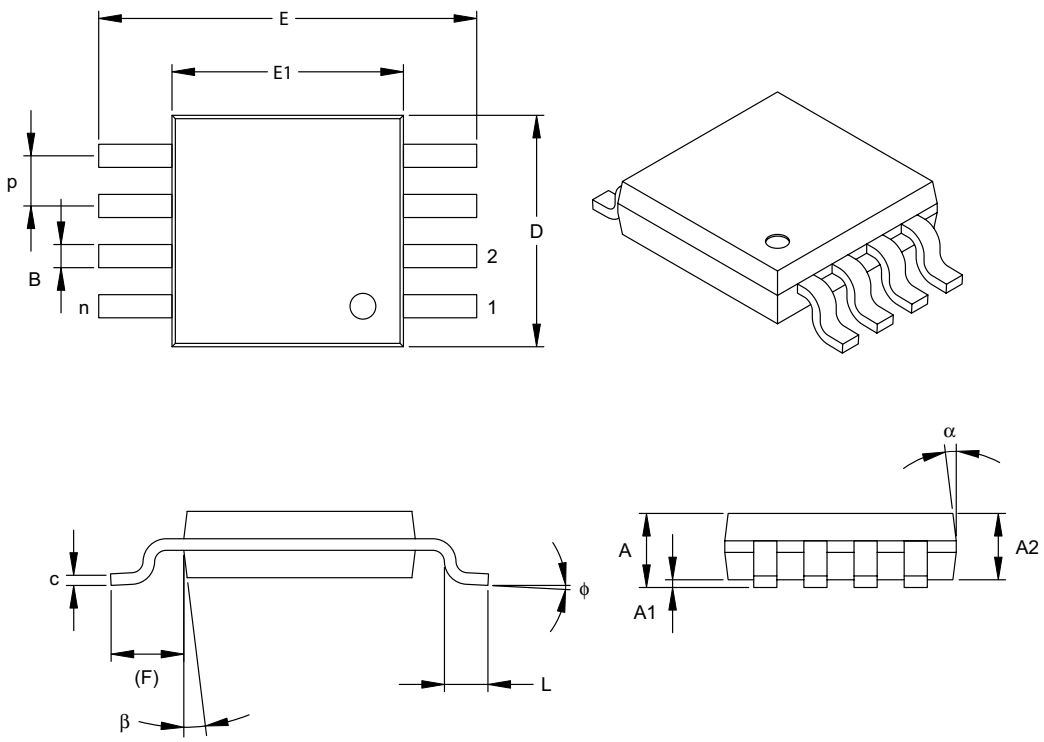
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	X
Device	Temperature Range	Package	Lead Finish

Device:	24AA52:	=	1.8V, 2 Kbit I^2C Serial EEPROM
	24AA52T:	=	1.8V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)
	24LCS52:	=	2.2V, 2 Kbit I^2C Serial EEPROM
	24LCS52T:	=	2.2V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)
Temperature Range:	I	=	-40°C to +85°C
Package:	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm), 8-lead
	MS	=	Plastic Micro Small Outline (MSOP), 8-lead
	MC	=	Micro Lead Frame (2x3 mm body), 8-lead
Lead Finish	Blank	=	Pb-free – Matte Tin **(see Note 1)**
	G	=	Pb-free – Matte Tin only

Examples:

a) 24AA52-I/P: Industrial Temperature, 1.8V, PDIP package

b) 24AA52-I/SN: Industrial Temperature, 1.8V, SOIC package

c) 24AA52T-I/MS: Tape and Reel, Industrial Temperature, 1.8V, MSOP package

d) 24LCS52-I/P: Industrial Temperature, 2.2V, PDIP package

e) 24LCS52-I/MC: Industrial Temperature, 2.2V, DFN package

f) 24LCS52T-I/MS: Tape and Reel, Industrial Temperature, 2.2V, MSOP package

Note 1: Most products manufactured after January 2005 will have a Matte Tin (Pb-free) finish. Most products manufactured before January 2005 will have a finish of approximately 63% Sn and 37% Pb (Sn/Pb).